REMARKS

Applicants respectfully request that this Amendement After Final Action to be admitted under 35 C.F.R. § 1.116.

Applicants submit that this Amendment After Final Action presents claims in better form for consideration. Moreover, applicants submit that this amendment responds to an argument that was first presented in the Office Action mailed 7/12/2007. Applicants submit that thus there are good and sufficient reasons why this amendment is necessary, why this amendment was not earlier presented, and why this amendment should be admitted now.

Claims 1-9, and 26-36 are pending in the present application.

Claim 28 is objected to because of informalities.

Claims 1-9, and 26-36 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,109,201 ("Petranovic").

Claims 6 and 33 have been canceled.

Claims 1, 26, 28 and 35 have been amended.

Applicants submit that claims 1, 26, and 35 have been amended to include limitations in previously presented claims 6, 33, and 31 respectively. Applicants submit that these limitations have been previously presented and have been examined by the Patent Office and thus do not require a new search.

Claim 28 is objected to because of informalities.

Claim 28 has been amended to correct the informalities. Applicants submit that the objection to claim 28 has been overcome in view of the amendment.

Claims 1-9, and 26-36 are rejected under 35 U.S.C. §102(b) as being unpatentable over Petranovic.

It is submitted that Petranovic does not render claims 1-5, 7-9, 26-32, 33-36 unpatentable under 35 U.S.C. §102(b).

Petranovic includes a disclosure of a method and apparatus for transforming the circuits comprising the critical path, thereby increasing the performance of the entire IC. The transformation is performed by segmenting, or blocking, the cells which make up the critical path. Then, each block is transformed, or replaced, with a resynthesized circuit to which both the digital 0 and digital 1 values are provided. The critical path is defined by the fact that the delay at each block is accumulated because each block has to wait for the output signal of the preceding block to use as its input signal. After the resynthesis of the blocks, none of the blocks need to wait for the output signal of its preceding block because each of the resynthesized blocks has the output for all possible inputs values (0 and 1). Thus, the signal delay at each block is not accumulated; rather, the only accumulated delay is the delay of the multiplexors used to select the correct output. The result is a dramatically reduced critical path delay (Petranovic Abstract).

It is submitted that Petranovic does not teach or suggest identifying a group of components associated with a critical signal in the system, creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state, and configuring the system to utilize a selector circuit on a target device to select an output of one of the first copy and the second copy in response to the critical signal, and removing unused components from the group of components.

On the contrary, Petranovic discloses a resynthesized circuit 60 that includes three blocks of cells, the original block 62, the first copy of the original block 64, and the second copy of the original block 66 (see Petranovic column 6, lines 20-29 and Figure 5). The blocks 62, 64, and 66 maintain all of their components whether used or unused. Petranovic discloses that the three blocks of cells 62, 64, and 66 are identical to each other and identical to the original block of cells, B_i 54, that the resynthesized circuit 60 is replacing (see Petranovic column 6, lines 22-24 and Figure 4 and 5). Petranovic does not teach or suggest removing unused components from the group of components.

The Office Action mailed 7/12/2007 states in part that

> As to claim 6, and 31 Petranovic et al. teach further comprising removing unused components from the group of components (see fig 2-5 col 5 line 3 to col 8 line 42).

(7/12/2007 Office Action, p. 3) (Emphasis Added).

Applicants submit that the cited text and figures make no reference to removing unused components or any components from the group of components. Applicants request that the Office clarify the relevance of the cited text.

In contrast, claim 1 states

> A method for designing a system on a target device utilizing field programmable gate arrays (FPGAs), comprising:
> identifying a group of components associated with a critical signal in the system;
> creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state;
> configuring the system to utilize a selector circuit on the target device to select an output of one of the first copy and the second copy in response to the critical signal; and
> removing unused components from the group of components.

(Claim 1 as amended) (Emphasis Added).

Claims 31 and 35 include the limitation of removing unused components from the group of components. Given that claims 2-5, and 7-9 depend from claim 1, and 36 depend from claim 35, it is likewise submitted that claims 2-5, 7-9, and 36 are also patentable under 35 U.S.C. §102(b) over Petranovic.

Applicants further submit that Petranovic does not teach or suggest determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations.

The Office Action mailed 7/12/2007 states in part that

> As to claim 8, 33, and 36 Petranovic et al. teach further comprising determining appropriate placement of the first copy and the second copy on the target device using an incremental

> placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations (see fig 4, fig 5 col 5 line 30 to col 6 line 47).

(7/12/2007 Office Action, pp. 3-4) (Emphasis Added).

Applicants submit that Petranovic does not provide any disclosure on how to resolve illegalities in placement. Furthermore the text cited by the Office, column 5, line 30 to column 6, line 47, does not appear to make any reference to moving components in the first and second copy not associated with a critical signal or any reference to preferred locations. Applicants request that the Office clarify the relevance of the cited text.

In contrast, claim 26 states

> A machine-readable medium having stored thereon sequences of instructions, the sequences of instructions including instructions which, when executed by a processor, causes the processor to perform:
>
> identifying a group of components associated with a critical signal in a system;
>
> creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state;
>
> configuring the system to utilize a selector circuit to select an output of one of the first copy and the second copy in response to the critical signal; and
>
> determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations.

(Claim 26 as amended) (Emphasis Added).

Claims 8 and 36 include similar limitations.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-5, 7-9, 26-32, and 3436 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12th day of October, 2007.

Lawrence M. Cho
Name

Signature